UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,885	10/12/2001	Hans Martin Buschbeck	H60-099 US	9683

21706 7590 03/08/2005

NOTARO AND MICHALOS
100 DUTCH HILL ROAD
SUITE 110
ORANGEBURG, NY 10962-2100

EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,885	BUSCHBECK ET AL	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *97-125* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *97-125* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 97-105, 109-110 and 115-123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuse et al (US 5,217,501) in view of Meyerson (US 5,906,680).

Fuse et al discloses a vertical wafer heat treatment apparatus for forming a film on a plurality of wafers stored in a wafer boat (Abstract). Fuse et al also discloses a process tube **10** is situated vertically and constitutes a vertical heat treatment unit and is used for chemical vapor deposition (CVD), this reads on applicant's subjecting the structural members to a CVD treatment to form a batch of CVD treatment members. Fuse et al also teaches wafers **20** are mounted on a boat **18** with each wafer kept horizontal and the wafers are arranged at

predetermined intervals in the vertical direction (col 3, ln 25-68), this reads on applicant's batch of disk-shaped structural members being in a horizontal position. Fuse et al also discloses a load lock chamber **0** below the process tube **10** and a vacuum is built in the load lock chamber (col 4, ln 4, ln 5-20). Fuse et al also teaches after the treatment is completed in the process tube **10**, the wafers are transferred from the boat **18** to a stocker in load lock chamber **44** (col 4, ln 20-40), this reads on applicant's removing the CVD treated members of the batch from the reactor.

Fuse et al does not teach an ultrahigh vacuum treatment reactor.

In a method of low-pressure chemical vapor deposition, Meyerson teaches ultra high vacuum is used in combination with a CVD system in order to provide initial base pressures less than 10^{-8} Torr to provide epitaxial growth of silicon films and allows batch processing to occur (col 4, ln 20-65 and col 5, ln 5-35). Meyerson also teaches epitaxial silicon are useful in order to reduce the dimensions of high performance integrated circuitry (col 1, ln 15-40). Meyerson also teaches a load chamber **12** and a means for providing an ultrahigh vacuum in a deposition tube of a CVD apparatus is essential to the deposition of epitaxial silicon layers of high quality onto a substrate (col 7, ln 1-10). Meyerson also teaches forming p-n junctions and MOS capacitors from the epitaxial silicon layer, this reads on applicants' manufacturing components or their intermediate products from the CVD treated members.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Fuse et al's CVD apparatus by employing an ultrahigh vacuum, as taught by Meyerson, to produce epitaxial silicon useful in the production of high performance integrated circuitry.

Referring to claims 98-100 and 102, the combination of Fuse et al and Meyerson teach subjecting the wafer carrier to a 30 minute bake in the load chamber prior to its transfer into the UHV section ('680 col 11, ln 45-67), this reads on applicant's pre-treating step, and a wafer carrier supporting the wafers in a horizontal position ('501 col 3, ln 55-67).

Referring to claims 101 and 104, the combination of Fuse et al and Meyerson teaches a load lock to eliminate contamination upon loading of the substrate prior to deposition ('680 col 4, ln 30-50) and the boat is baked at approximately 100°C while the loading chamber is pumped down to 10^{-7} Torr ('680 col 7, ln 0-65), this reads on applicants' cleaning the structural members because contamination is removed.

Referring to claim 103, the combination of Fuse et al and Meyerson teaches wafer stockers **71** and **72** for loading and unloading a boat one by one ('501 col 4, ln 25-40).

Referring to claim 105, the combination of Fuse et al and Meyerson teaches transporting from the load lock chamber to the CVD tube, which is located above the load lock chamber, this reads on applicant's linear path.

Referring to claims 109-110, the combination of Fuse et al and Meyerson teaches pumping hydrogen gas into the deposition chamber during the loading of the boat **30** ('680 col 7, ln 1-67), this reads on applicant's providing a gas flow during the loading step.

Referring to claim 115, the combination of Fuse et al and Meyerson teaches heating the reactor to a deposition temperature ('680 claim 16).

Referring to claim 116, the combination of Fuse et al and Meyerson teaches a hot wall furnace **32** around a reaction tube **34** ('680 col 6, ln 15-35 and Fig 1), this reads on applicant's providing a further atmosphere around an atmosphere in the ultrahigh vacuum reactor.

Referring to claim 117, the combination of Fuse et al and Meyerson teaches a first atmosphere in a deposition chamber **10** and a second atmosphere in a load chamber **12** ('680 Fig 1).

Referring to claim 118, the combination of Fuse et al and Meyerson is silent to the second atmosphere is established to be a lower pressure then the first atmosphere. This feature is inherent to the combination of Fuse et al and Meyerson because the combination of Fuse et al and Meyerson teaches a silane deposition source is introduced into the deposition chamber ('680 col 12, ln 40-67), thereby increase the pressure of the deposition to greater than the load chamber.

Referring to claim 119, the combination of Fuse et al and Meyerson teaches separate pumping apparatuses for the load chamber and the UHV furnace ('680 Fig 1), this reads on applicant's separately pumping the first and second atmospheres.

Referring to claim 120, the combination of Fuse et al and Meyerson teaches a pumping means **20** is used to evacuate the loading chamber and a pumping means **38** to evacuate the tube **34** ('680 col 5, 35 to col 6, ln 55), this reads on applicant's establish the first and second atmospheres substantially independent of each other.

Referring to claim 121, the combination of Fuse et al and Meyerson teaches opening a valve **16**.

Referring to claim 122-123, the combination of Fuse et al and Meyerson teaches substrate are baked for about 5 minutes in a hydrogen atmosphere at the deposition temperature, followed by stopping the flow of hydrogen and starting a silicon gas source flow ('680 col 7, ln 45-67), this reads on applicant's allowing the structural members to reach thermal equilibrium.

Referring to claim 124, the combination of Fuse et al and Meyerson teaches heating the boat **18**.

3. Claims 106-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuse et al (US 5,217,501) in view of Meyerson (US 5,906,680), as applied to claims 97-105, 109-110 and 115-123 above, and further in view of Fukui et al (US 5,755,938).

The combination of Fuse et al and Meyerson teach all of the limitations of claim 106, as discussed previously, except the structural members are subjected to a reactive, low energy plasma treatment process.

In a method of forming a film by chemical vapor deposition, note entire reference, Fukui et al teaches a substrate cleaning step, where contaminants and impurities such as H_2O, CO_2 or native oxide on the surface of a substrate is removed. Fukui et al also teaches a mixed gas atmosphere of Argon and Hydrogen is created in a deposition chamber and RF power is supplied to a first electrode to thereby perform a plasma cleaning and the ion energy applied is in the range of 10-20 eV (col 7, ln 10-30), overlapping ranges are held to be obvious (MPEP 2144.05). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Fuse et al and Meyerson with Fukui et al's plasma cleaning process to remove contaminants and impurities such as H_2O, CO_2 or native oxide on the surface of a substrate.

Referring to claim 108, the combination of Fuse et al, Meyerson and Fukui et al teaches an atmosphere of hydrogen.

4. Claims 111 and 113 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuse et al (US 5,217,501) in view of Meyerson (US 5,906,680), as applied to claims 97-105, 109-110 and 115-123 above, and further in view of Olsen et al (US 6,021,152).

The combination of Fuse et al and Meyerson teach all of the limitations of claim 111, as discussed previously, except the average temperature and the temperature distribution in a reaction volume of the CVD process are measured and controlled.

In a method of controlling temperature uniformity in a CVD process, note entire reference, Olsen et al teaches a reflector plate in a reaction chamber to achieve a uniform temperature distribution across a substrate (Abstract and col 1, ln 15-65) and the power of various lamps **56, 66** can be controlled independently in response to temperature sensors arranged in proximity to the substrate **20** (col 4, ln 10-60). Olsen et al also teaches the advantages are applicable to batch wafer processing furnaces (col 3, ln 40-55). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Fuse et al and Meyerson with Olsen et al's CVD reactor with sensors and reflector plates to achieve a uniform temperature distribution within the chamber and across the wafer to improve the uniformity of the deposited films (col 1, ln 25-55).

5. Claims 112 and 114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuse et al (US 5,217,501) in view of Meyerson (US 5,906,680) and Olsen et al (US 6,021,152), as applied to claims 111 and 113 above, and further in view of Stollenwerk et al (US 6,150,030).

The combination of Fuse et al, Meyerson and Olsen et al teach all of the limitations of claim 112, as discussed previously, except controlling at least one of the average temperature and the temperature distribution by at least one of open loop or negative loop control.

In a method of semiconductor deposition, Stollenwerk et al teaches a heating and/or cooling arrangement, which is adjustable in an open loop controlled or in a negative feedback controlled manner to set a substrate temperature (col 6, 5-15). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Fuse et al, Meyerson and Olsen et al by controlling temperature with a open loop or a negative feedback controller, as taught by Stollenwerk et al, because such control mechanisms are conventionally used in the art to control temperature.

6. Claim 125 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fuse et al (US 5,217,501) in view of Meyerson (US 5,906,680) as applied to claims 97-105, 109-110 and 115-123 above, and further in view of Kobayashi (JP 07-022430), an English Abstract has been provided.

The combination of Fuse et al and Meyerson teach all of the limitations of claim 125, as discussed previously, except providing thermal sensors at a support for carrying each structural member to the reactor and sensing the temperature of each structural member at the support using the thermal sensor.

In a method of manufacturing a semiconductor, Kobayashi teaches monitoring a temperature change and temperature control of semiconductor substrates are performed by a temperature monitoring thermoelectric couple to enhance the uniformity of a heat treatment.

Kobayashi also teaches providing the thermoelectric couple in the boat of a furnace to be used in a heat treatment process (Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Fuse et al and Meyerson by using a thermoelectric couple to monitor the temperature of the substrates and enhance uniformity of a heat treatment, as taught by Kobayashi.

Response to Arguments

7. Applicant's arguments, see page 12 of the remarks, filed 8/8/2003, with respect to rejection in view of the combination of Chu ('134) and Tsai ('102) have been fully considered and are persuasive. The rejection of claims 49 and 50 has been withdrawn.

8. Applicant's arguments with respect to claims 97-125 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nasser-Faili et al (US 6,013,191) teaches thermocouples and a feedback loop are well known and suitably control a power supply to maintain a desired temperature (col 5, ln 15-35).

Yao et al (US 5,746,512) teaches a vertical wafer boat and thermocouples are used to detect temperature (col 2, ln 50 to col 3, ln 50).

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS
March 2, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER